CLAIMS

What is claimed is:

1. An imaging error diffusion apparatus comprising:

a first thread having an error input and a pixel input and producing an error output; and

at least one other thread each having a pixel input and an error input, the at least one other thread producing an error output in response to the error output of the first thread.

2. The apparatus as claimed in claim 1, wherein the at least one other thread is at least two threads, where each of the other threads has an error input coupled to an error output of another thread.

3. The apparatus as claimed in claim 1, wherein the first thread receives error data of a previous row and pixel data of a current row and the at least one other thread receives error data of the current row and pixel data of a subsequent row.

4. The apparatus as claimed in claim 1, wherein the apparatus is included within an image signal processor.

5. The apparatus as claimed in claim 1, wherein the apparatus is included within a digital media processor.

6. The apparatus as claimed in claim 1, wherein a total number of the first thread and the at least one other threads is equal to or greater than a number of stages in an error diffusion hardware pipeline.

7. The apparatus as claimed in claim 6, wherein the total number of the first thread and the at least one other threads is equal to the number of stages in the error diffusion hardware pipeline.

8. The apparatus as claimed in claim 7, wherein the total number of the threads and the number of the stages is three.

9. The apparatus as claimed in claim 1, wherein each of the first thread and the at least one other threads execute concurrently.

10. The apparatus as claimed in claim 1, wherein the first thread has a second error input.

11. The apparatus as claimed in claim 10, wherein each of the at least one other threads has a second error input.

12. The apparatus as claimed in claim 1, wherein each of the at least one other threads has a second error input.

13. An imaging error diffusion method comprising:

receiving at a first thread an error input and a pixel input and producing an error output; and

receiving at a second thread a pixel input and the error output of the first thread and producing an error output in response to the error output of the first thread.

14. The method of claim 13, further comprising the first thread calculating an error value for a current pixel based on the pixel input, the error input and at least one other previously calculated error value within the first thread.

15. The method of claim 13, further comprising receiving at a third thread a pixel input and the error output of the second thread and producing an error output in response to the error output of the second thread.

16. The method of claim 13, wherein the first thread and the second thread execute concurrently.

17. The method of claim 13, wherein the first thread receives a second error input.

18. The method of claim 17, wherein the second thread receives a second error input.

19. The method of claim 13, wherein the second thread receives a second error input.

20. A system comprising

a memory; and

a processor coupled to the memory; and

an imaging error diffusion apparatus comprising:

a first thread having an error input and a pixel input and producing an error output; and

at least one other thread each having a pixel input and an error input, the at least one other thread producing an error output in response to the error output of the first thread.

21. The system as claimed in claim 20, wherein the error output of the first thread is not stored in memory.

22. The system as claimed in claim 20, wherein the error output of the first thread is not stored in any memory external to the threads.

23. The system as claimed in claim 20, wherein a total number of the first thread and the at least one other threads is equal to or greater than a number of stages in an error diffusion hardware pipeline included in the processor.

24. The system as claimed in claim 23, wherein the total number of the first thread and the at least one other threads is equal to the number of stages in the error diffusion hardware pipeline.

25. The apparatus as claimed in claim 24, wherein the total number of the threads and the number of the stages is three.

26. The apparatus as claimed in claim 20, wherein each of the first thread and the at least one other threads execute concurrently.

27. The system as claimed in claim 20, wherein the first thread has a second error input.

28. The system as claimed in claim 27, wherein each of the at least one other threads has a second error input.

29. The apparatus as claimed in claim 20, wherein each of the at least one other threads has a second error input.